SEP 02 2005 PATENT & TRADEMARK OFFICE

Fig. 1
(PRIOR ART)

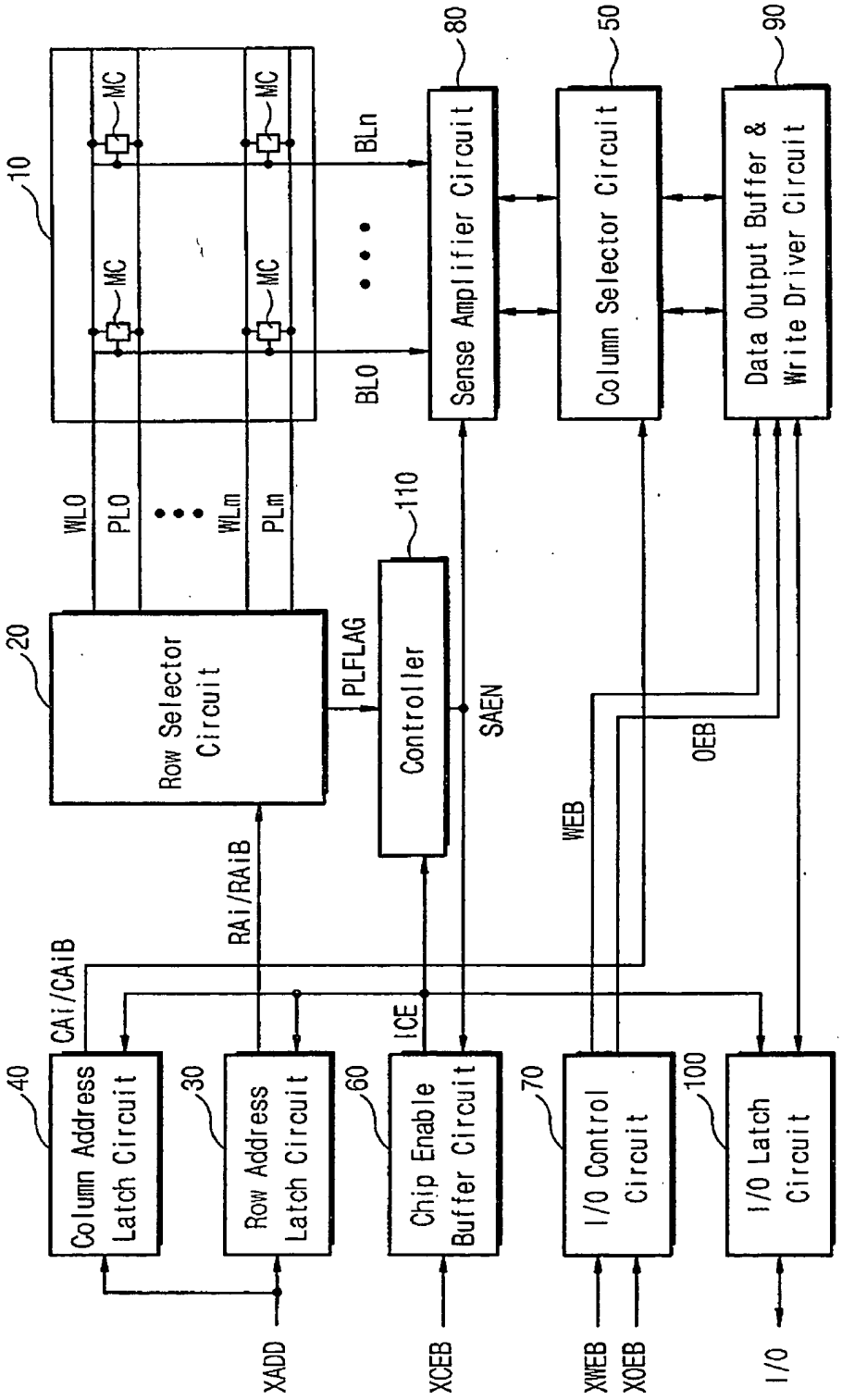

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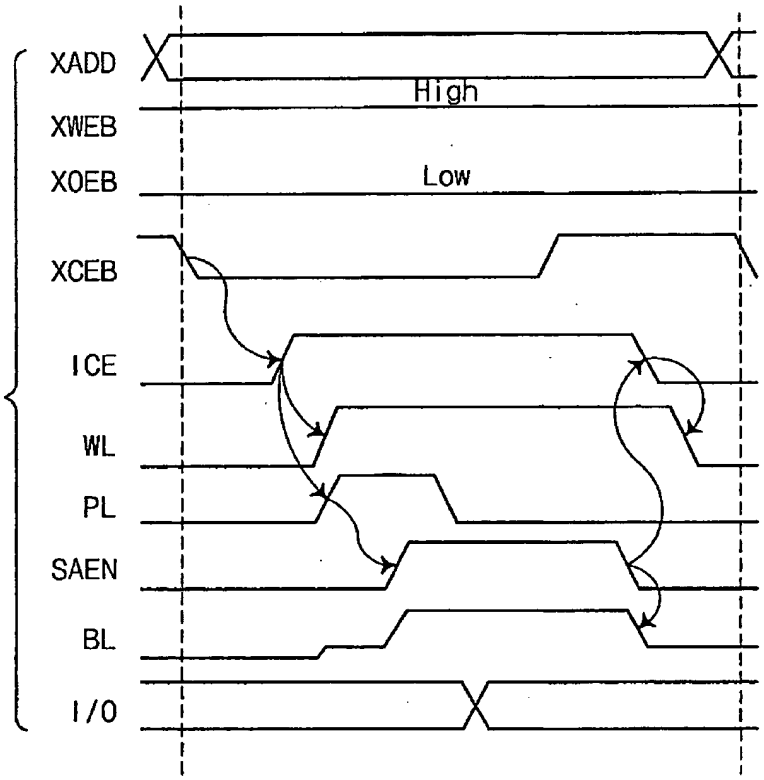
Fig. 2

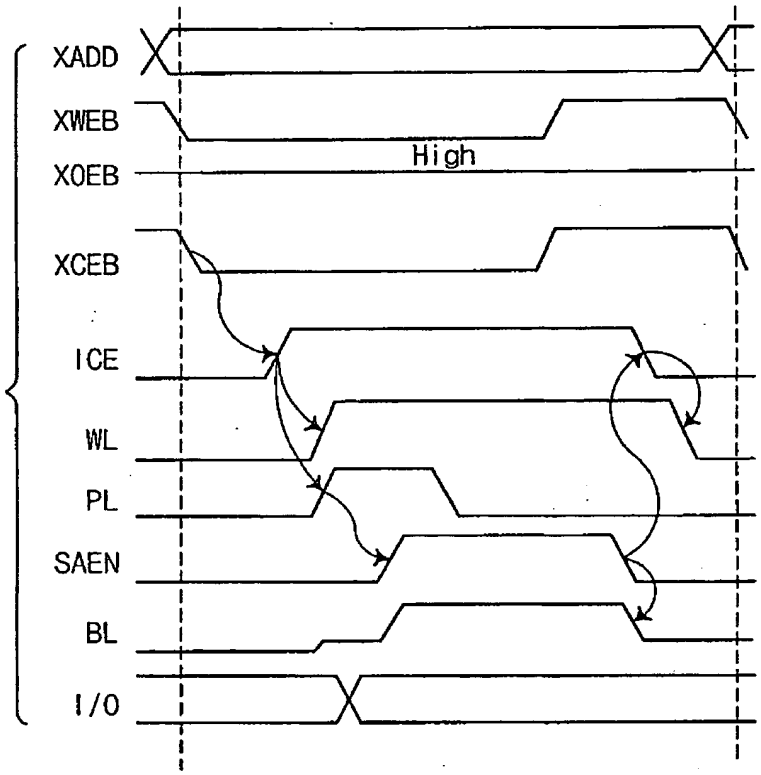
(PRIOR ART)

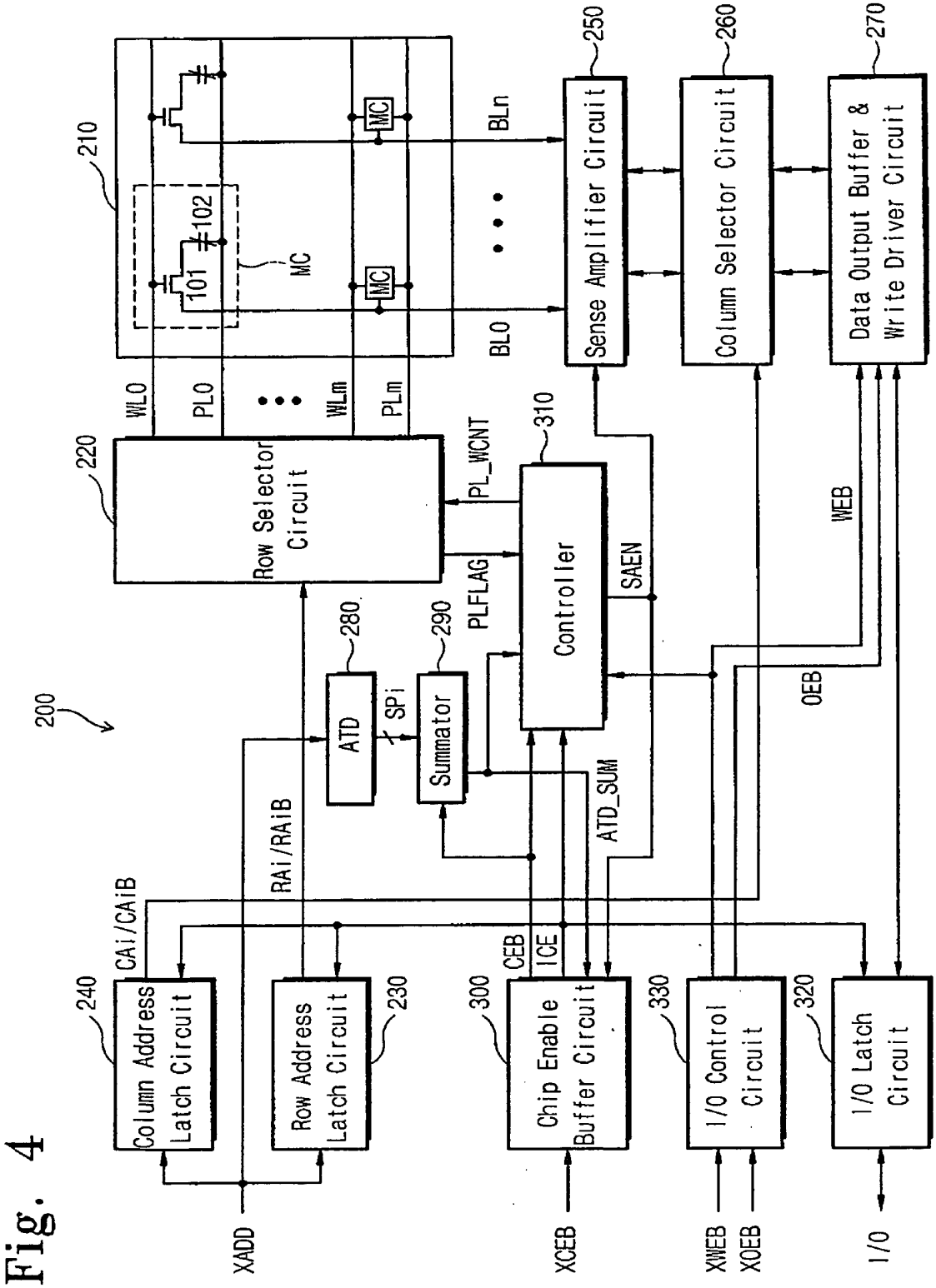


PAGE 5/11 * RCVD AT 9/2/2005 6:13:43 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/24 * DNIS:7464000 * CSID:5032744622 * DURATION (mm-ss):03-26

Fig. 3

(PRIOR ART)

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330
MC
101
102
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PL0
WLm
PLm
BLn
BL0
Row Selector Circuit
Sense Amplifier Circuit
Column Selector Circuit
Data Output Buffer & Write Driver Circuit
Controller
PL_WCNT
PLFLAG
SAEN
WEB
OEB
ATD
SPi
Summator
ATD_SUM
RAi/RAiB
CAi/CAiB
Column Address Latch Circuit
Row Address Latch Circuit
CEB
ICE
Chip Enable Buffer Circuit
I/O Control Circuit
I/O Latch Circuit
XADD
XCEB
XWEB
XOEB
I/O

Fig. 4

Fig. 5

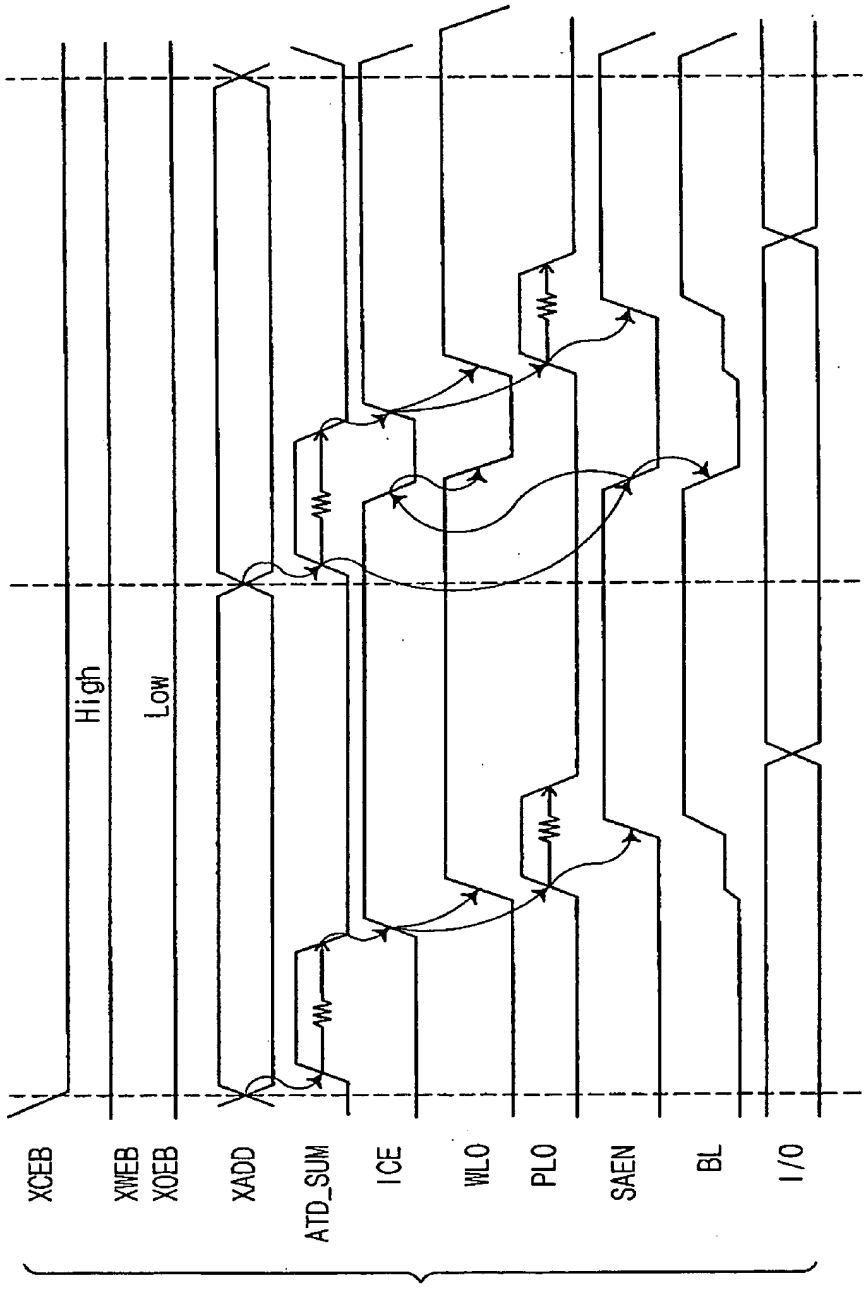
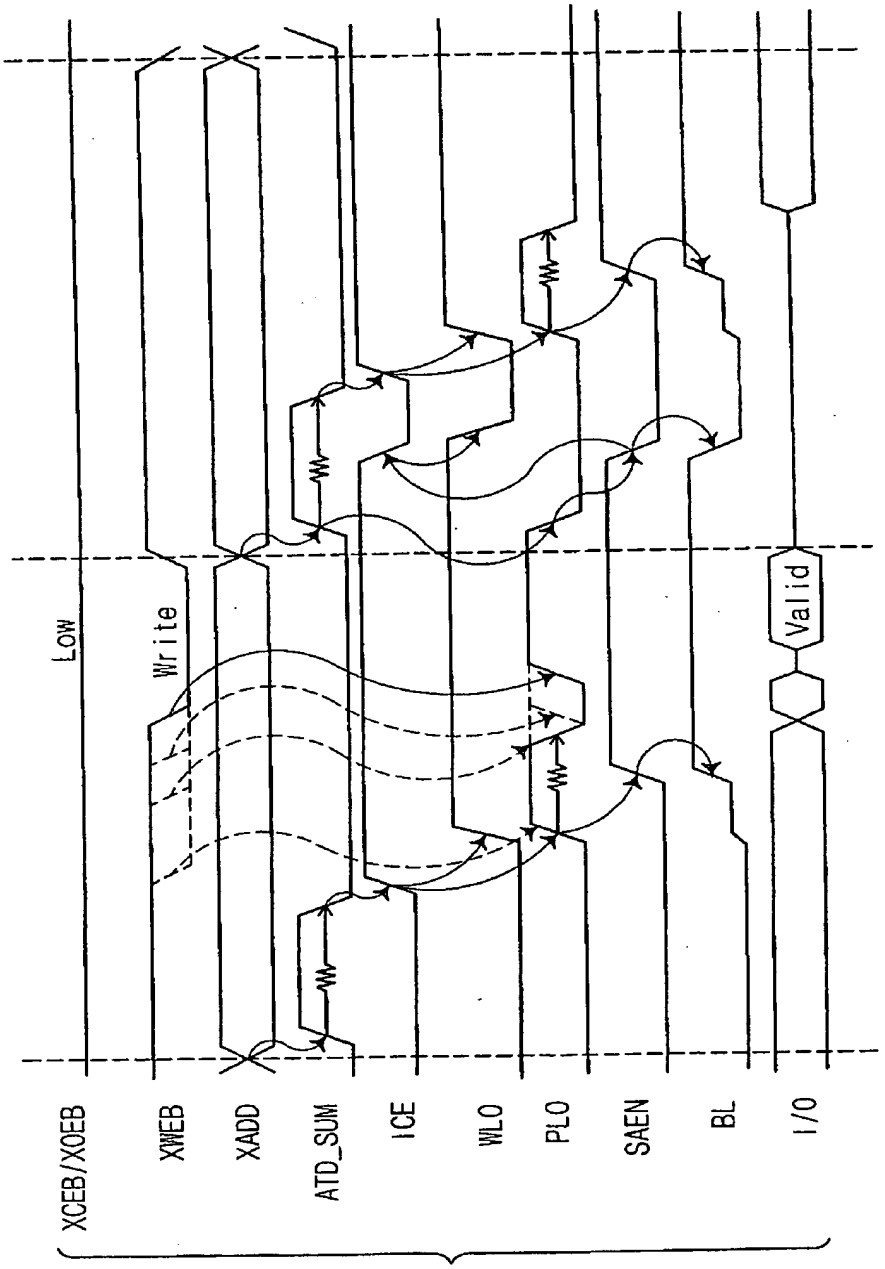


Fig. 6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